IN THE CLAIMS

1. (Currently Amended) A data transmission device comprising:

a clock generation circuit generating a clock signal;

a jitter generator generating jitter in the clock signal based on a setting signal, which sets a present condition of the jitter; and

a data transmission circuit transmitting data in sync with the clock signal including the jitter.

2. (Previously Presented) The data transmission device according to claim 1, wherein

the jitter generator adjusts an amount of modulation or the frequency of the jitter

3. (Previously Presented) The data transmission device according to claim 1, wherein

the jitter generator generates at least one of a sinusoidal jitter and a random jitter in the clock signal.

4. (Currently Amended) The data transmission device according to claim 2, wherein

the jitter generator ~~supply circuit~~ generates at least one of a sinusoidal jitter and a random jitter in the clock signal.

5. (Currently Amended) An I/O interface circuit comprising:

a clock generation circuit generating a first clock signal;

a jitter generator generating jitter in the first clock signal based on a setting signal, which sets a present condition of the jitter; and

a data transmission circuit transmitting data in sync with the first clock signal including the jitter.

6. (Previously Presented) The I/O interface circuit according to claim 5, wherein

the jitter generator adjusts an amount of modulation or the frequency of the jitter.

7. (Previously Presented) The I/O interface circuit according to claim 5, wherein

the jitter generator generates at least one of a sinusoidal jitter and a random jitter in the first clock signal.

8. (Previously Presented) The I/O interface circuit according to claim 6, wherein

the jitter generator generates at least one of a sinusoidal jitter and a random jitter in the first clock signal.

9. (Currently Amended) The I/O interface circuit according to claim 5, further comprising:

a data reception circuit receiving the transmitted data, wherein

the clock generation circuit also supplies a second clock signal to the data reception circuit,

the data transmission circuit comprises:

pattern generation circuit generating a data pattern for a jitter resistance test, and

transmission circuit allowing the data pattern generated by the pattern generation circuit to be transmitted in sync with the first clock signal, and

the data reception circuit comprise:

reception circuit allowing the data pattern transmitted ~~received~~ by the transmission circuit to be received in sync with the second clock signal, and

pattern comparison circuit comparing the data pattern received by the reception circuit with an expectation value to output a comparison result.

10. (Previously Presented) The I/O interface circuit according to claim 9, further comprising:

measurement result storage circuit associatively storing the comparison result delivered by the pattern comparison circuit and information on an amount of modulation or the frequency of the jitter.

11. (Currently Amended) The I/O interface circuit according to claim 9, further comprising:

a jitter generator control circuit controlling the jitter generator to vary [[the]] an amount of modulation [[and/or]] or the frequency of the jitter in accordance with the comparison result delivered by the pattern comparison circuit and a measurement procedure for the jitter resistance.

12. (Currently Amended) The I/O interface circuit according to claim [[9]] 11, wherein

the jitter generator control circuit controls the jitter generator so as to vary the amount of modulation of the jitter when the comparison result delivered by the pattern comparison circuit indicates a match and to vary the frequency of the jitter when the comparison result delivered by the pattern comparison circuit indicates a mismatch.

13. (Currently Amended) The I/O interface circuit according to claim 9, wherein

the pattern generation circuit in the data transmission circuit ~~further~~ comprises:

a circuit including data of a contiguous sequence of 0s or 1s in the data pattern, and

the pattern comparison circuit in the data reception circuit ~~further~~ comprises

a first circuit detecting the data of a contiguous sequence of 0s or 1s having been received, and

a second circuit forcing the comparison result to indicate a match when the first circuit detects the data of [[a]] the contiguous sequence of 0s or 1s having been received.

14. (Currently Amended) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit replaces part of the data pattern with data of a contiguous sequence of 0s or 1s, thereby allowing the data pattern to include the data of [[a]] the contiguous sequence of 0s or 1s.

15. (Currently Amended) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit inserts data of a contiguous sequence of 0s or 1s into a midpoint of the data pattern, thereby allowing the data pattern to include the data of [[a]] the contiguous sequence of 0s or 1s.

16. (Previously Presented) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit further comprises a circuit adjusting a cycle in a case of data of a contiguous sequence of 0s or 1s being included in the data pattern in that cycle.

17. (Previously Presented) The data transmission device according to claim 1, further comprising:

a selector selecting the clock signal including the jitter based on a control signal.

18. (Currently Amended) The data transmission device according to claim 1, further comprising:

a first voltage controlled oscillator receiving the clock signal including the jitter; and

a second voltage controlled oscillator receiving a signal from the jitter generator.

19. (Previously Presented) The I/O interface circuit according to claim 5, further comprising:

a selector selecting the first clock signal including the jitter based on a control signal.

20. (Currently Amended) The I/O interface circuit according to claim 5, further comprising:

a first voltage controlled oscillator receiving the first clock signal including the jitter; and

a second voltage controlled oscillator receiving a signal from the jitter generator.

21. (New) A transfer system comprising:

a data transmission part transmitting data in sync with sync a clock signal, and including a clock generator circuit generating the clock signal, a jitter generator generating jitter in the clock signal based on a setting signal which sets a present condition of the jitter and a data transmission circuit transmitting the data in sync with the clock signal including the jitter; and

a data reception part receiving the data and the clock signal including the jitter, and measuring a transfer condition.